**An Efficient Implementation of Floating Point Multiplier**

**Abstract**

In this paper we describe an efficient implementation of an IEEE 754 single precision floating point multiplier targeted for Xilinx Virtex-5 FPGA. VHDL is used to implement a  
technology-independent pipelined design. The multiplier implementation handles the overflow and underflow cases. Rounding is not implemented to give more precision when using  
the multiplier in a Multiply and Accumulate (MAC) unit. With latency of three clock cycles the design achieves 301 MFLOPs. The multiplier was verified against Xilinx floating point  
multiplier core.

**LANGUAGE USED:**

* Vhdl/verilog

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis